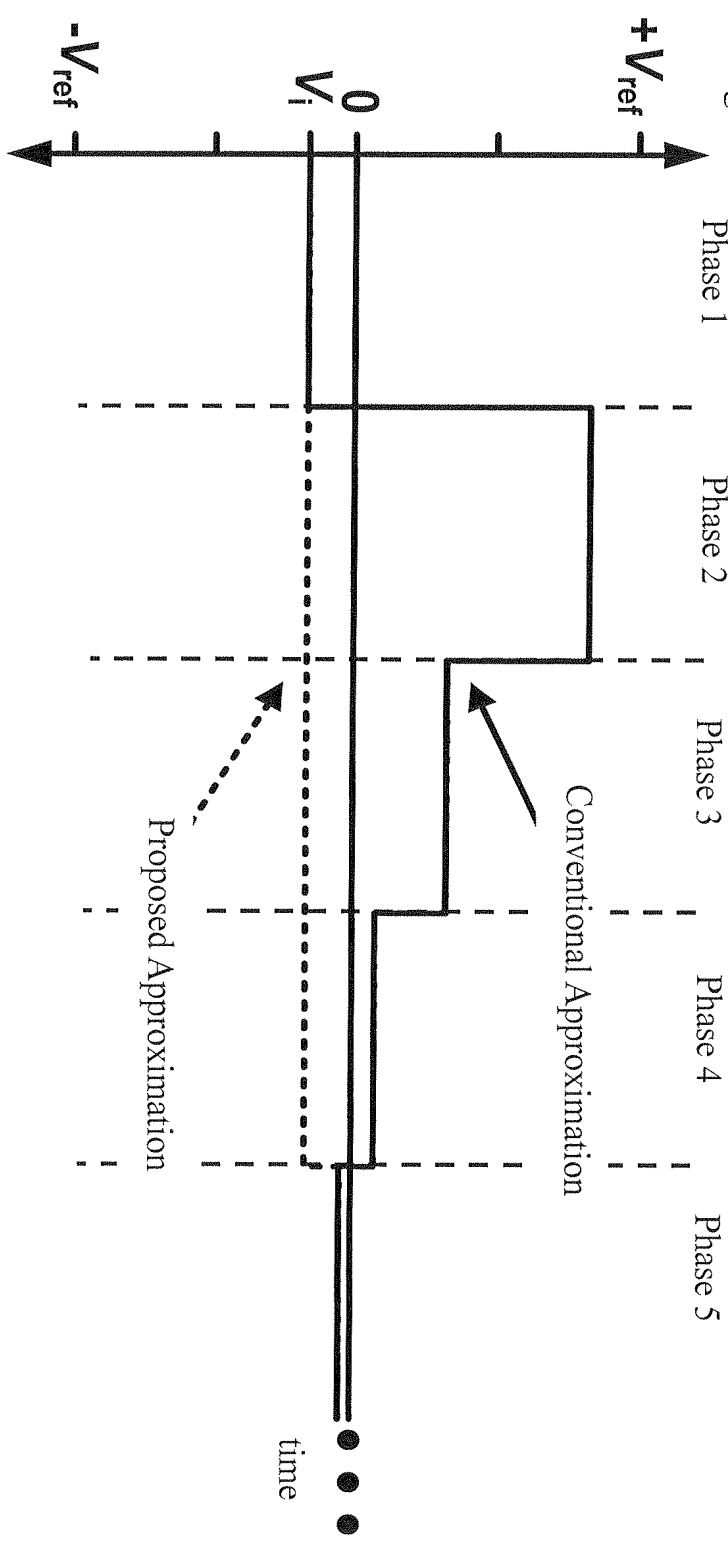
voltage
+Vref
0
Vi
-Vref
Phase 1
Phase 2
Phase 3
Phase 4
Phase 5
Conventional Approximation
Proposed Approximation
time

Fig. 1

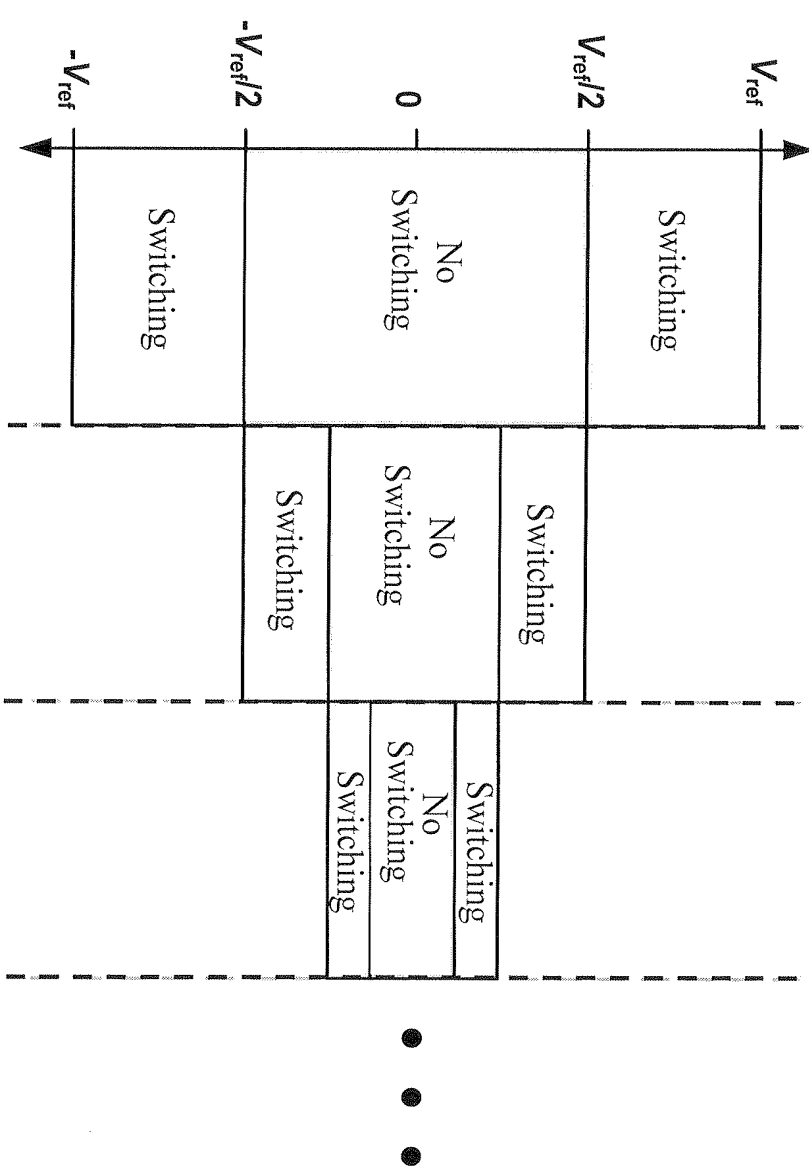
voltage
V_{ref}
$V_{ref}/2$
0
$-V_{ref}/2$
$-V_{ref}$
Phase 1
Phase 2
Phase 3
Switching
No Switching
Switching
No Switching
Switching
Switching
No Switching
Switching

Fig. 2

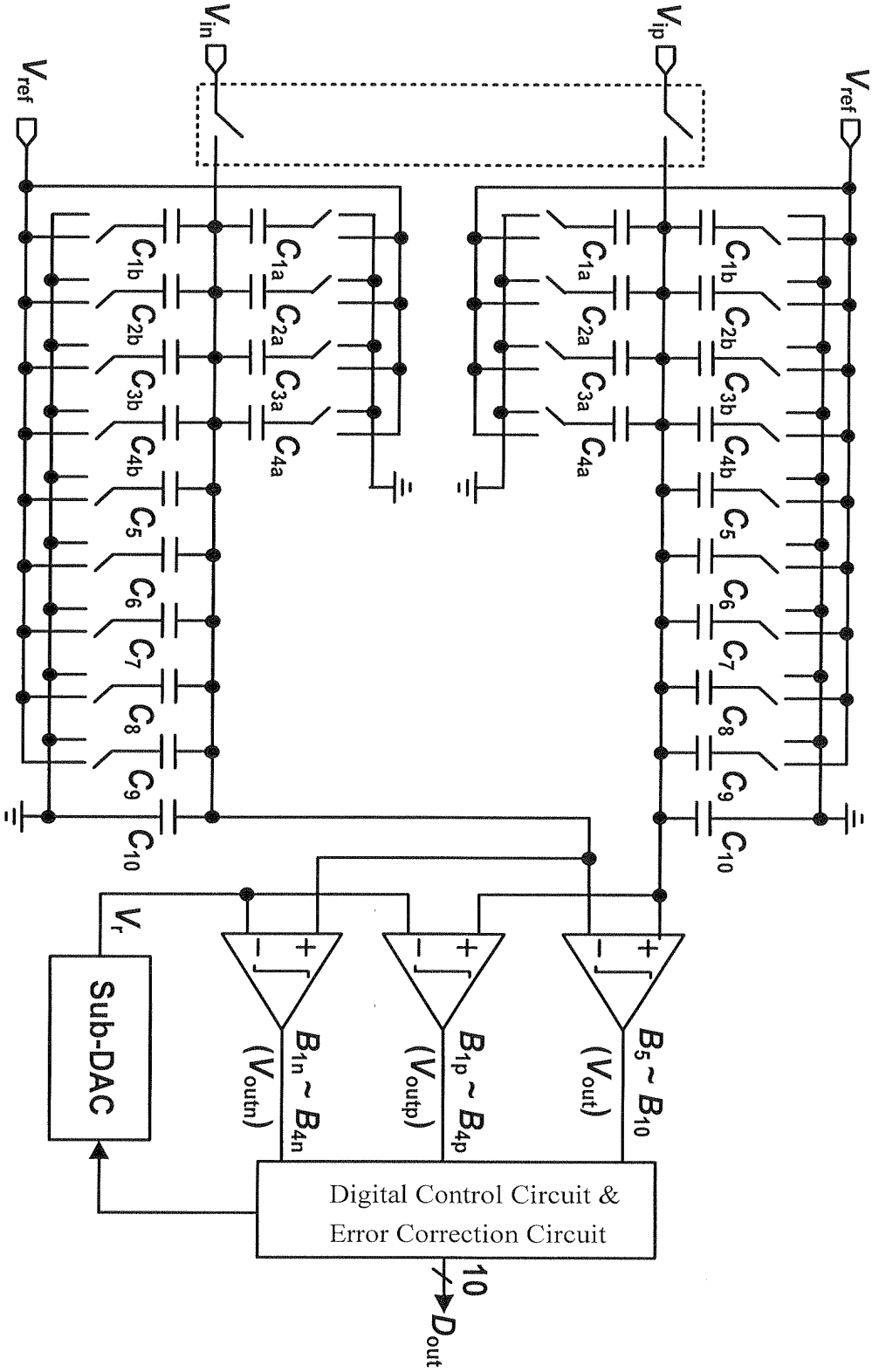
V_{ref}
V_{ip}
V_{in}
V_{ref}
C_{1a}
C_{1b}
C_{2a}
C_{2b}
C_{3a}
C_{3b}
C_{4a}
C_{4b}
C_5
C_6
C_7
C_8
C_9
C_{10}
V_r
Sub-DAC
$B_{1n} \sim B_{4n}$ (V_{outn})
$B_{1p} \sim B_{4p}$ (V_{outp})
$B_5 \sim B_{10}$ (V_{out})
Digital Control Circuit & Error Correction Circuit
10
D_{out}

Fig. 3

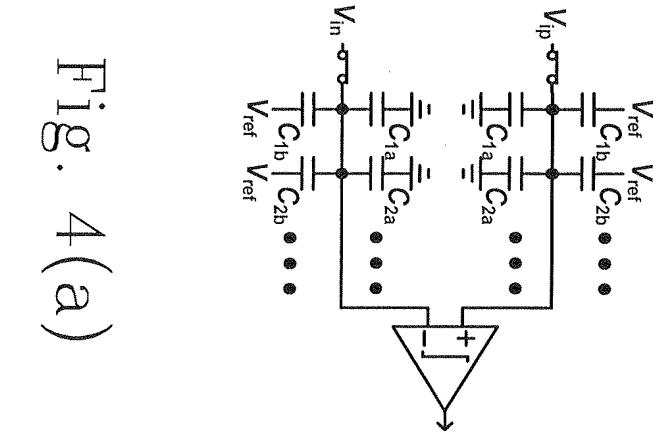

Fig. 4(a)

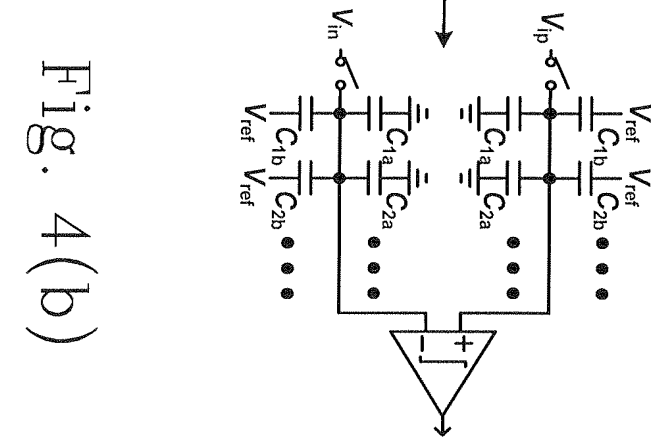

Fig. 4(b)

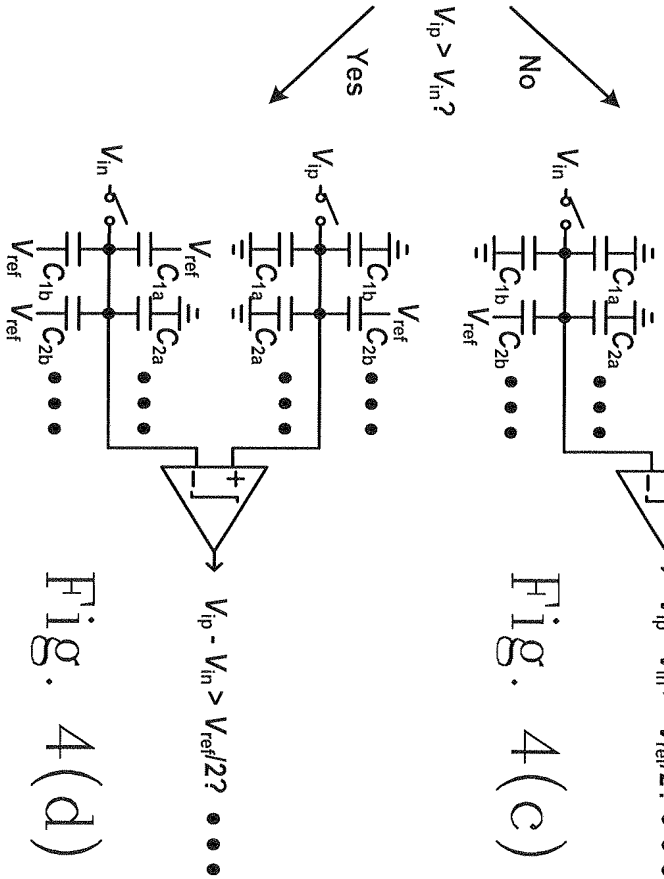

Fig. 4(c)

Fig. 4(d)

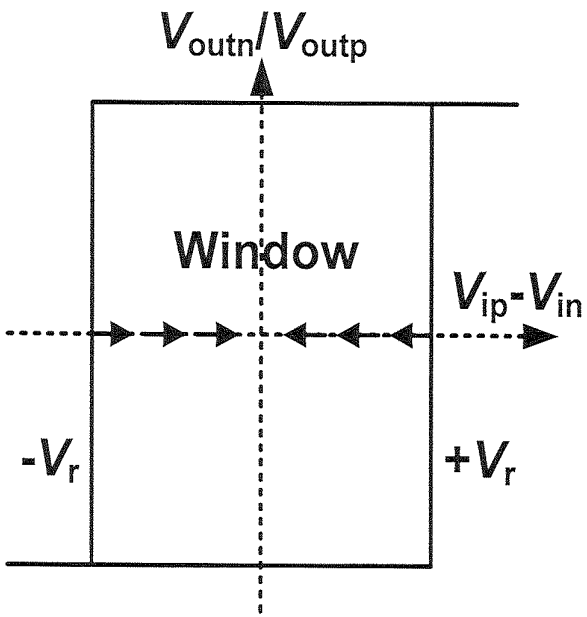
V_{outn}/V_{outp}
Window
V_{ip}-V_{in}
-V_r
+V_r

Fig. 5(a)

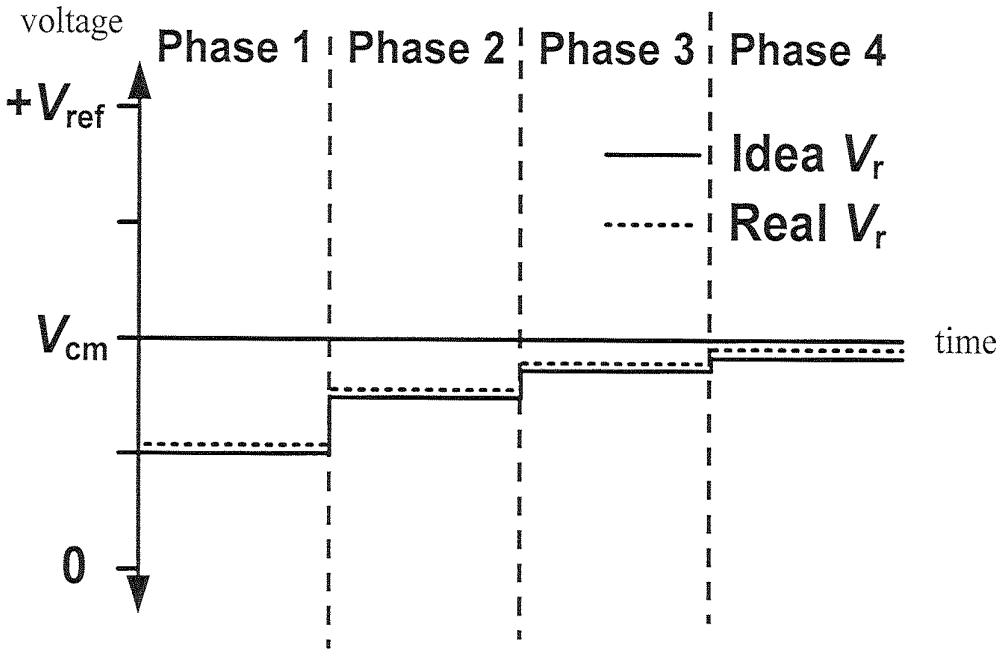
voltage
Phase 1
Phase 2
Phase 3
Phase 4
+V_{ref}
Idea V_r
Real V_r
V_{cm}
time
0

Fig. 5(b)

				B_5	B_6	B_7	B_8	B_9	B_{10}
	$\overline{B_{1n}}$	$\overline{B_{2n}}$	$\overline{B_{3n}}$	$\overline{B_{4n}}$					
+	B_{1p}	B_{2p}	B_{3p}	B_{4p}					
D_1	D_2	D_3	D_4	D_5	D_6	D_7	D_8	D_9	D_{10}

Fig. 6(a)

	B_{xp}	$\overline{B_{xn}}$	State
$V_{ip} > V_r$ $V_{in} < V_r$	1	1	Switching
$V_{ip} > V_r$ $V_{in} > V_r$	1	0	No Switching
$V_{ip} < V_r$ $V_{in} > V_r$	0	0	Switching

Fig. 6(b)

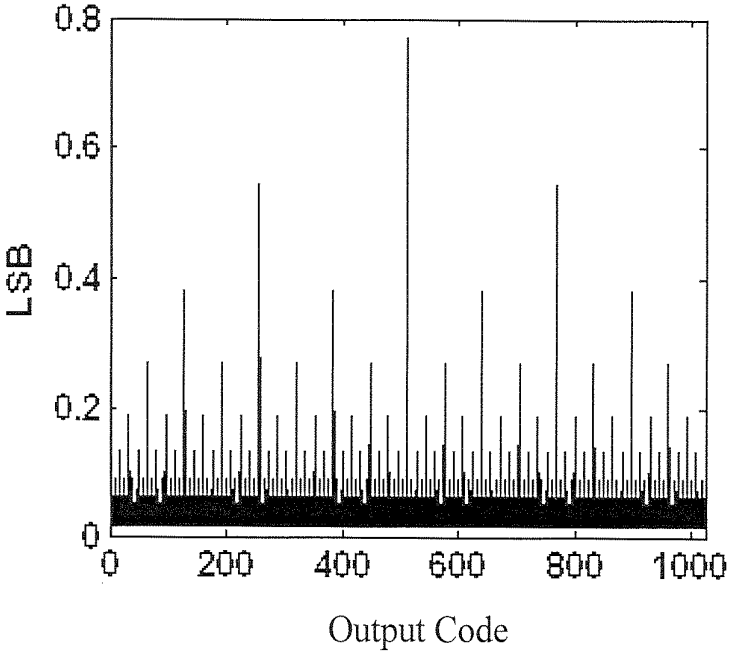

Fig. 7(a)
(Prior Art)

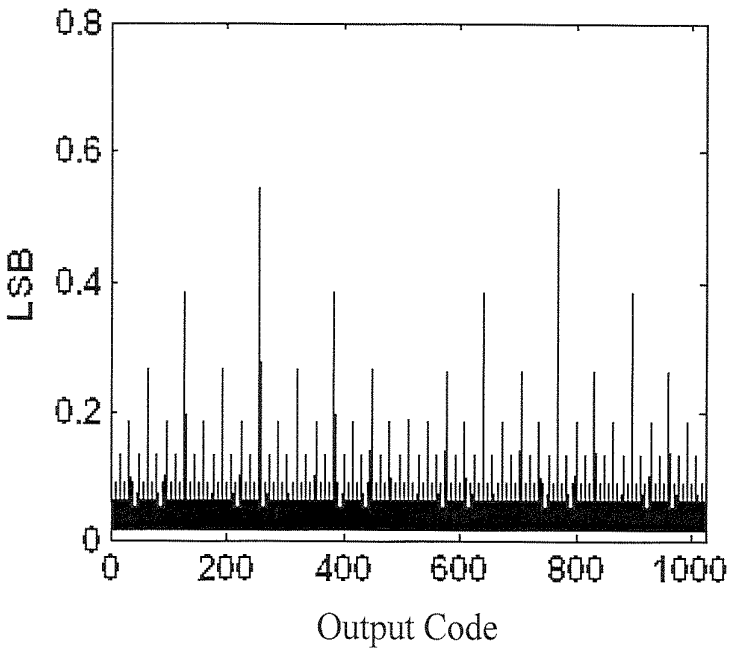

Fig. 7(b)

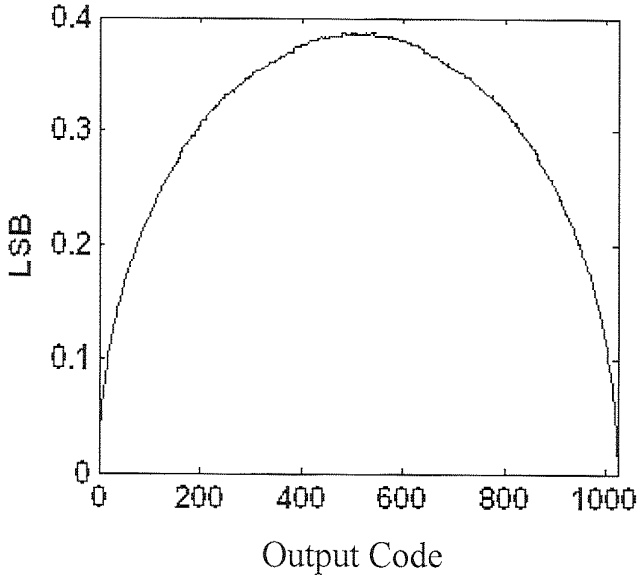

Fig. 7(c)
(Prior Art)

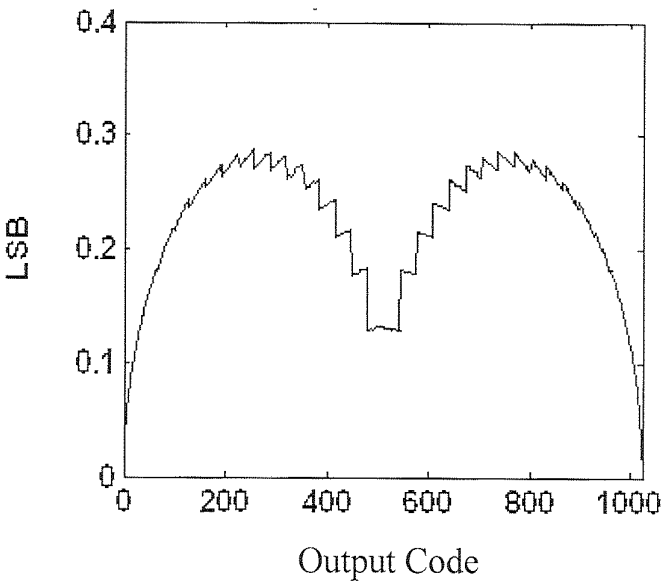

Fig. 7(d)