WHAT IS CLAIMED IS:

1. A successive approximation analog-to-digital converter, comprising:

a positive and a negative input terminals;

a capacitor array having at least one capacitor with a first and a second terminals, and a plurality of bits, counting from a most significant bit (MSB) to a least significant bit (LSB), wherein each of the plurality of bits electrically connects with the at least one capacitor, the first terminal electrically connects with one of the positive input terminal and the negative input terminal, and the second terminal switchably connects with a first and a second reference voltage sources to selectively receive one of a first reference voltage and a second reference voltage;

a first comparator receiving an adjustable third reference voltage and electrically connected to the positive input terminal, wherein the second terminal of each the at least one capacitor is configured to be switched when the voltage on the positive terminal is larger than a third reference voltage; and

a second comparator receiving the third reference voltage and electrically connected to the negative input terminal, wherein the second terminal of the at least one capacitor is configured to be switched when the voltage on the negative terminal is less than a negative value of the third reference voltage.

2. A converter according to Claim 1 further comprising a first and a second bootstrapped switches, a digital control circuit, an error correction circuit, a third comparator electrically connected to the positive and the negative input terminals and a sub-digital to analog converter (sub-DAC), wherein the positive and the negative input terminals receive an input

signal, the input signal is a differential signal, the first and the second bootstrapped switches are respectively connected between the positive input terminal and the third comparator, and the negative input terminal and the third comparator for completely passing the differential signal through the positive and the negative input terminals, the third comparator is used to adjust the potential level of each of the remaining bits except for the predetermined number of the plurality of bits, the sub-DAC generates the adjustable third reference voltage, the digital control circuit and the error correction circuit electrically connect with the first, the second and the third comparators and the sub-DAC, and the digital control circuit and the error correction circuit generate a digital code matched to the input signal.

3. A converter according to Claim 2, wherein the third comparator has a comparison result, and the comparison result of the third comparator and a binary search algorithm are used to adjust the potential level of each of the remaining bits except for the predetermined number of the plurality of bits to generate the digital code, the third reference voltage is adjusted to one half of a present value thereof when the comparison result is generated, and the third reference voltage is restored to an initial value after all of the predetermined number of the plurality of bits are adjusted once.

4. A converter according to Claim 1, wherein the predetermined number is K, K is an integer, N is a total number of output bits of the converter, K is not larger than N, and each of the 1^{st} to the K^{th} bits has four capacitors, each of which has an equivalent capacitance.

5. A converter according to Claim 4 further comprising K 3-bit full adders, wherein:

each of the K full adders is used to generate at least one digital code of the 1^{st} to the $(K+1)^{th}$ bits, the K^{th} full adder adds a first output signal of the first comparator, an inverse value of a second output signal of the second comparator and a third output signal of the $(K+1)^{th}$ bit to generate the digital code of the $(K+1)^{th}$ bit when the $(K+1)^{th}$ bit is computed;

when the K^{th} bit is computed, the $(K-1)^{th}$ full adder adds a first output signal of the first comparator, an inverse value of a second output signal of the second comparator and a carry signal of the K^{th} full adder to generate the digital code of the K^{th} bit and this procedure is repeated until the 2nd bit is computed;

the 1^{st} full adder adds a first output signal of the first comparator, an inverse value of a second output signal of the second comparator and a carry signal of the 2nd full adder to generate the digital code of the 2^{nd} bit; and

a carry signal of the 1^{st} adder is the digital code of the 1^{st} bit.

6. A successive approximation analog-to-digital converter, comprising:

a capacitor array having at least one capacitor with a first and a second terminals, and a plurality of bits, each of which is connected to the at least one capacitor, wherein the first terminal receives an input signal, and the second terminal selectively receives one of a first and a second reference voltages; and

a first comparator receiving an adjustable third reference voltage and a first voltage value generated by the input signal, wherein a connection of the second terminal of each the capacitor of the capacitor array is

switched when the first voltage value is larger than the third reference voltage.

7. A converter according to Claim 6 further comprising a second comparator receiving the third adjustable reference voltage and a second voltage value generated by the input signal, wherein a connection of the second terminal of each the capacitor of the capacitor array is switched when the second voltage value is larger than the third reference voltage.

8. A converter according to Claim 7 further comprising a positive and a negative input terminals receiving the input signal, a first and a second bootstrapped switches, a digital control circuit, an error correction circuit, a third comparator electrically connected to the positive and the negative input terminals and a sub-digital to analog converter (sub-DAC), wherein the first and the second comparators are used to adjust respective potential levels of a predetermined number of the plurality of bits from a most significant byte (MSB) to a least significant byte (LSB), the input signal is a differential signal, the first and the second bootstrapped switches are respectively connected between the positive input terminal and the third comparator, and the negative input terminal and the third comparator for completely passing the differential signal through the positive and the negative input terminals, the third comparator is used to adjust the respective potential level of each of the remaining bits except for the predetermined number of the plurality of bits, the sub-DAC generates the adjustable third reference voltage, the digital control circuit and the error correction circuit electrically connect with the first, the second and the third comparators and the sub-DAC, and the digital

control circuit and the error correction circuit generate a digital code matched to the input signal.

9. A converter according to Claim 8, wherein a comparison result of the third comparator and a binary search algorithm are used to adjust the potential level of each of the remaining bits except for the predetermined number of the plurality of bits, the third reference voltage is adjusted to one half of a present value thereof when the comparison result is generated, and the third reference voltage is restored to an initial value when all of the predetermined number of the plurality of bits are adjusted once.

10. A converter according to Claim 8, wherein the predetermined number is K, K is an integer, N is a total number of output bits of the converter, K is not larger than N, and each of the 1^{st} to the K^{th} bits has four capacitors, each of which has an equivalent capacitance.

11. A converter according to Claim 10 further comprising K 3-bit full adders.

12. A method for adjusting a successive approximation analog-to-digital converter having at least one capacitor with a first and a second terminals, comprising steps of:

providing a plurality of bits, each of which is connected to the at least one capacitor, wherein the first terminal receives an input signal, and the second terminal selectively receives one of a first and a second reference voltages;

comparing a voltage generated by the input signal with a third reference voltage;

switching a connection of the second terminal of each the capacitor when there is one of the two following cases where the first case is the voltage is larger than the third reference voltage while the second case is the voltage is less than a negative value of the third reference voltage; and

adjusting the third reference voltage every time after a voltage comparison with the third reference voltage is executed.

13. A method according to Claim 12, wherein the adjusting step further comprises a step of: adjusting the third reference voltage to one half of a present value thereof every time after the comparison is executed, and then restoring the third reference voltage to an initial value thereof until each of a predetermined number of the plurality of bits has been adjusted once.

14. A method according to Claim 12, wherein the input signal is a differential signal, the converter comprises a positive and a negative input terminals receiving the differential signal, the voltage is a voltage difference between the positive input terminal and the negative input terminal and the converter is used to generate a digital code matched to the differential signal.