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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the **PATENT APPLICATION** of:	
	Chang et al.
Application No.:	13/052,462
Confirmation No.:	6528
Filed:	March 21, 2011
For:	SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER HAVING AUXILIARY PREDICTION CIRCUIT AND METHOD THEREOF
Group:	2819
Examiner:	Joseph J. Lauture

Our File: DEENCK-PT002
Date: November 20, 2012

7 Pages VIA FACSIMILE TO: 1-571-273-8300

RESPONSE TO EXAMINER REQUEST FOR CLARIFICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This responds to the October 24, 2012 telephone call from the examiner.

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REMARKS/ARGUMENTS

The examiner indicated in the telephone call that certain contents of the description may contain errors: The features "the adjustable third reference voltage, Vr" and "the positive input terminal" have been shown in Fig. 3 and are described in the specification: "a first comparator receiving an adjustable third reference voltage Vr and electrically connected to the positive input terminal" (see paragraph [0022], Line 14) and "the first terminal electrically connects with one of the positive input terminal (receiving Vip) and the negative input terminal (receiving Vin)" (see paragraph [0022], Line 9). Furthermore, a first comparator that is electrically connected to the positive input terminal can also be clearly observed in Fig. 3" and "On reviewing figure 3, Vr does appear connected to the negative (not positive) terminal."

The applicants respectfully submit that the features "A successive approximation analog-to-digital converter, comprising: a positive and a negative input terminals...a first comparator receiving an adjustable third reference voltage and electrically connected to the positive input terminal" as recited in Claim 1 mean that the positive and the negative input terminals are the positive and the negative input terminals of the proposed successive approximation analog-to-digital converter respectively, rather than the positive and the negative input terminals of the first comparator. The first comparator receives the adjustable third reference

voltage Vr and the first comparator is electrically connected to the positive input terminal of the converter instead of the assertion that the adjustable third reference voltage Vr is electrically connected to the inverting terminal of the first comparator since the inverting terminal of first comparator is not recited in Claim 1 and is not mentioned in Paragraph [0022].

Thus, the questioned contents in Paragraph [0022] of the specification "a first comparator receiving an adjustable third reference voltage Vr and electrically connected to the positive input terminal" are correct when these contents are compared with Claim 1 and Fig. 3. As shown in Fig. 3, the first comparator (which is the middle one of the three comparators) receives the adjustable third reference voltage Vr and the first comparator is electrically connected to the positive input terminal (which receives Vip as shown in Fig. 3) instead of that the adjustable third reference voltage Vr is electrically connected to the non-converting terminal of the first comparator (note that in the first comparator as recited in Claim 1, there is an "and" between "receiving the adjustable third reference voltage" and "electrically connected to the positive input terminal" and this indicates that the first comparator is electrically connected to the positive input terminal of the proposed converter rather than that the adjustable third reference voltage Vr is electrically connected to the non-inverting terminal of the first comparator). In Fig. 3, Vr is indeed received by the inverting terminal of the first comparator, but which input

terminal receives the adjustable third reference voltage Vr is not the issue, and the adjustable third reference voltage Vr being received by the first comparator is. The above-mentioned relationship of connection regarding Vr, the first comparator and the positive input terminal of the converter as recited in Claim 1 can be observed in Fig. 3. As for the second question regarding, "the first terminal electrically connects with one of the positive input terminal (receiving Vip) and the negative input terminal (receiving Vin)", which are described as: "a capacitor array having at least one capacitor with a first and a second terminals, and a plurality of bits, counting from a most significant bit (MSB) to a least significant bit (LSB), wherein each of the plurality of bits electrically connects with the at least one capacitor (Cia=2C(i+1)a, i=1-3; Cja=Cjb, j=1-4; CK=2C(k+1), k=5-8; C4a=C5, C9=C10), the first terminal electrically connects with one of the positive input terminal (receiving Vip) and the negative input terminal (receiving Vin)" (See paragraph [0022], Lines 4-11). These contents are also recited in Claim 1 as "a capacitor array having at least one capacitor with a first and a second terminals, and a plurality of bits, counting from a most significant bit (MSB) to a least significant bit (LSB), wherein each of the plurality of bits electrically connects with the at least one capacitor, the first terminal electrically connects with one of the positive input terminal and the negative input terminal, and the second terminal...". Thus, the first terminal described in Paragraph [0022], Line 9 of the present specification refers to the first

terminal of the at least one capacitor included in the capacitor array, wherein the at least one capacitor has a first terminal and a second terminal, and the first terminal of the at least one capacitor connects with one of the positive input terminal (which receives Vip as shown in Fig. 3) of the proposed converter and the negative input terminal (which receives Vin as shown in Fig. 3) of the proposed converter.

The above-mentioned description regarding the first terminal of the at least one capacitor included in the capacitor array can be observed from Fig. 3, and these capacitors are presented in the form of a pair. Observed from the upper part of Fig. 3, it can be seen that each of the capacitors C_1a, Clb, C_2a, C_2b,...C10 has a terminal connected with the positive input terminal (receiving Vip). In the lower part of Fig. 3, each of the capacitors C_1a, Clb, C_2a, C_2b,...C10 has a terminal connected with the negative input terminal (receiving Vin). Accordingly, the aforementioned descriptions regarding the first terminal of the at least one capacitor included in the capacitor array are correct that at least one terminal of the capacitors connects with one of the positive input terminal (receiving Vip) and the negative input terminal (receiving Vin).

Based on the above-mentioned descriptions and analyses, one could draw a conclusion that the above-mentioned descriptions in Paragraph [0022] of the present specification questioned by the examiner are correct and can be clearly understood by one with an ordinary skill in the field.

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For the above mentioned reasons, the applicants respectfully request withdrawal of the objection under 37 CFR 1.83(a).

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Conclusion

In view of the foregoing remarks, the applicants respectfully request reconsideration of the application, and allowance at an early date would be appreciated.

Should the examiner have any questions or comments, the examiner is invited to contact the undersigned by telephone so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,

Chang et al.

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