WHAT IS CLAIMED IS:

1. A sense amplifier, comprising:

a first switch having a first terminal, a second terminal and a control terminal receiving a first bias;

a second switch having a first terminal electrically connected to the first terminal of the first switch, a second terminal and a control terminal receiving a second bias;

a third switch having a first terminal, a second terminal electrically connected to the first terminal of the first switch and a control terminal receiving a third bias;

a holding path including the second switch; and

a fourth switch controlling a turn-on and a turn-off of the holding path and having a first terminal electrically connected to the second terminal of the second switch, a second terminal and a control terminal receiving a sensing signal.

2. A sense amplifier according to Claim 1, wherein the holding path pre-charges a memory, the first bias is different from the second bias, and the second bias equals to the third bias.

3. A sense amplifier according to Claim 1 further comprising a sensing and pre-charging path having a sensing node, and a capacitor having a first and a second terminals, wherein the holding path pre-charges a memory, the first bias and the second bias are a first bit line bias and a second bit line bias respectively, the first terminal of the capacitor electrically connected to the sensing node and the first terminal of the third switch, and the second terminal of the capacitor connects a ground, the memory includes a bit line and a storage cell connected to the bit line, when the first and the third switches are turned on and a potential value of the sensing node has a relatively low value, the storage cell is in a conductive status, when the first and the third switches are turned on and the

potential value of the sensing node has a relatively high value, the storage cell is in a non-conductive status, the potential value of the sensing node forms the sensing signal, when the second and the fourth switches are turned on, the holding path is conductive, and the bit line is pre-charged to a first predetermined potential value.

4. A sense amplifier according to Claim 3 further comprising a fifth to a eighth switches, each of which has a first, a second and a control terminals, a latch circuit has a first and a second terminals and two cross-connected inverters, and a strobe path, wherein the first terminal of the fifth switch connects the sensing node, the second terminal of the fifth switch connects the second terminal of the fourth switch and the first terminal of the latch circuit, the first terminal of the sixth switch receives a power supply voltage, the second terminal of the sixth switch connects the first terminal of the seventh switch, the second terminal of the seventh switch connects the second terminal of the latch circuit, the first terminal of the eighth switch connects the second terminal of the first switch, the second terminal of the eighth switch connects the bit line, the control terminal of the eight switch receives a bit line select signal such that the eight switch is selectively connected to a specific bit line, the potential value of the second terminal of the latch circuit is transferred to the sensing node when the fifth switch is turned on, the seventh switch is used to detect whether the sensing and pre-charging path is conductive, the sensing and pre-charging path connects the eight switch, the first switch, the third switch and the control terminal of the seventh switch, the holding path connects the eighth switch, the first switch, the second switch, the fourth switch and the latch circuit, and the strobe path

connects the sixth switch, the seventh switch and the second terminal of the latch circuit.

5. A sense amplifier according to Claim 4 further comprising a ninth switch having a first, a second and a control terminals, wherein the first terminal of the ninth switch connects the second terminal of the fourth switch, the second terminal of the ninth switch connects the second terminal of the fifth switch, the control terminal of the ninth switch receives a fourth bias controlling the conducting time of the holding path, each of the fourth, the sixth and the seventh switches is a PMOS, and each of the first to the third, the fifth, the eighth and the ninth switches is an NMOS.

6. A sense amplifier according to Claim 4 further comprising a diode having an anode and a cathode and controlling the conduction time of the holding path, wherein the cathode of the diode is electrically connected to the second terminal to the fourth switch, and the anode of the diode is electrically connected to the second terminal of the fifth switch.

7. A sense amplifier according to Claim 3, wherein the memory is a flash memory, the bit line connects a drain gate select (DGS), a source gate select (SGS) and plural storage cells.

8. A sense amplifier according to Claim 7, wherein the flash memory is one of a NAND flash memory and a NOR flash memory.

9. A method for a sense amplifier, comprising steps of:

forming a holding path including a main control switch and a holding switch; and

providing an auxiliary control switch to control a turn-on and a turn-off of the holding path,

wherein the sense amplifier is the sense amplifier as claimed in Claim 5, the main control switch is the first switch, the holding switch is the second switch, the auxiliary control switch is the fourth switch, and the method further comprises steps of:

causing the holding path to be conductive when the second and the fourth switches are turned on; and

causing the sensing and pre-charging path to be conductive when the first and the third switches are turned on, and pre-charging the bit line to the first predetermined value via the sensing and pre-charging path, wherein the potential value of the sensing node is a potential value of the storage cell.

10. A method according to Claim 9, wherein the memory further comprises a word line electrically connected to the storage cell, and the step of causing conductive the holding path further comprises steps of:

causing the value of first bias of the first switch to drop to zero to separate the bit line and the sense amplifier;

adding a second predetermined potential value to the word line, wherein the storage cell generates a current and has a relatively low potential value when the storage cell is read and is in a conductive status and the storage cell does not generate any current and has a relatively high potential value when the storage cell is read and is in a non-conductive status;

causing the sensing node to be pre-charged to a value of the power supply voltage, a charge sharing status between the sensing node and the bit line occurs such that a potential value of the sensing node becomes equal to that of the bit line when the read storage cell is in the conductive status, and the potential value of the sensing node remains at the power supply voltage when the read storage cell is in the non-conductive status; and

causing the potential value of the second terminal of the latch circuit to be transferred to the sensing node so as to output the relatively high potential and the relatively low potential when the fifth switch is turned on.

11. A sense amplifier, comprising:

a switch circuit having a main control switch, a sensing switch and a holding switch, wherein the three switches have a first bias, a second bias, and a third bias respectively; and

an auxiliary control switch electrically connected to the holding switch to control an operation of the holding switch.

12. A sense amplifier according to Claim 11 further comprising a sensing and pre-charging path including the main control switch and the sensing switch, sensing a potential value of a storage cell connected to a bit line of a memory and generating a sensing signal according to the potential value, wherein the switch circuit includes the main control, the sensing and the holding switches clamping the bit line according to the first to the third bias respectively.

13. A sense amplifier according to Claim 12 further comprising a holding path including the holding switch and an auxiliary control switch electrically connected to the holding switch and receiving the sensing signal to control a turn-on and a turn-off of the holding path accordingly.

14. A sense amplifier according to Claim 12, wherein the memory is a flash memory.

15. A method for a sense amplifier, comprising steps of:

forming a holding path including a main control switch and a holding switch; and

providing an auxiliary control switch to control a turn-on and a turn-off of the holding path.

16. A method according to Claim 15 further comprising steps of:

forming a sensing and pre-charging path including the main control switch and a sensing switch;

sensing a potential value of a storage cell connected to a bit line of a memory via the sensing and pre-charging path; and

generating a sensing signal according to the potential value.

17. A method according to Claim 16, wherein the step of providing an auxiliary control switch further comprising a step of controlling the turn-on and the turn-off of the holding path according to the sensing signal.