Amendments to the Specification:

Please replace the present Paragraphs [0006] - [0007], [0011] - [0014], and [0044] with the following Paragraphs in accordance with the examiner's suggestions.

[0006] In Fig. 1 (a), a NAND flash memory 10 and a sense amplifier including a clamping circuit 21 are shown. The NAND flash memory 10 includes a DGS (drain gate select), a SGS (source gate select) and plural storage cells. The sense amplifier includes switches sw1-sw3 and sw5-sw8, a capacitor C, and a latch circuit including two cross-connected inverters IN1 and IN2. The switches sw1-sw3 are used to clamp the bit line and receive the first to the third bit line clamping biases BLC1, BLC2 and BLC3 respectively. The switch sw5 receives the signal LPC. When the switch sw5 is turned on, the potential value of the second terminal of the latch circuit SENB is transferred to the node SEN. The sense amplifier further includes a sensing and pre-charging path sw8-sw1-sw3-sw7, a holding path sw8-sw1-sw2-the latch circuit and a strobe path sw6-sw7-SENB. The sensing and pre-charging path is used to sense a potential value of a specific storage cell connected to a bit line in the NAND flash memory at the node SEN so as to show whether the storage cell is in a conductive status or a non-conductive status. The storage cell generates a current and has a relatively low potential value when the storage cell is in a conductive status, and the storage cell does not generate any current and has a relatively high potential value when the storage cell is in a non-conductive status. Due to a charge sharing status, the node SEN will show the potential value of the specific storage cell being read out. The holding path pre-charges the bit line to a first pre-determined potential value. The switch sw6 of the strobe path receives a

power supply voltage VDD and a control signal STR for controlling the strobe path, and the switch sw7 of the strobe path is used to judge whether the sensing and pre-charging path is in a conductive status, or in a non-conductive status. Fig. 1(a) further shows a metal bit line is connected with the bit line connected to the DGS and the plural storage cells, and switch sw8 (a bit line select) at node MBL, and shows a common source line (CSL).

[0007] Fig. 1(b) shows simulation waveforms of potential values of signals BLC1, BLC2, BLC3 and LPC, and potential values of nodes MBL, SEN, ~~and~~ SENA, STR and SENB: v(BLC1), v(BLC2), v(BLC3), v(LPC), v(MBL), v(SEN), ~~and~~ v(SENA), v(STR) and v(SENB) as shown in the circuit diagram of Fig. 1(a). In the marked region, a large voltage drop is shown. Such a voltage drop results from the design of having three bit line clamping biases BLC1, BLC2, BLC3 and two cascode paths. One of the two cascode paths is from BLC1 to BLC3, and the other one is from the BLC1 to BLC2 as shown in Fig. 1(a). Due to that VDD is not big enough at the marked region with bigger voltage drops, it is necessary to boost the voltage of SEN to ensure that the devices on the two cascode paths would be operated in the saturation region so as to result in the extra losses of raising the voltage, and this is what should be improved. Fig. 1(b) is during pre-charging of the nodes SENA and SEN by the latch.

[0011] According to a ~~the~~ first aspect of the present invention, a sense amplifier comprises a first switch having a first terminal, a second terminal and a control terminal receiving a first bias, a second switch having a first terminal electrically connected to the first terminal of the first switch, a second terminal and a control terminal receiving a second bias, a third switch having a first terminal, a second

terminal electrically connected to the first terminal of the first switch and a control terminal receiving a third bias, a holding path including the second switch, and a fourth switch controlling a turn-on and a turn-off of the holding path and having a first terminal electrically connected to the second terminal of the second switch, a second terminal and a control terminal receiving a sensing signal.

[0012] According to a ~~the~~ second aspect of the present invention, a sense amplifier having a clamping circuit comprises a main control switch having a first bias to decide whether or not the clamping circuit should operate, a sensing switch electrically connected to the main control switch and having a second bias, and a holding switch electrically connected to the main control switch and the sensing switch, and having a third bias, wherein the first bias is different from the second bias, and the second bias equals to the third bias.

[0013] According to a ~~the~~ third aspect of the present invention, a sense amplifier comprises a switch circuit having a main control switch, a sensing switch and a holding switch, wherein the three switches have a first bias, a second bias, and a third bias respectively, and an auxiliary control switch electrically connected to the holding switch to control an operation of the holding switch.

[0014] According to a ~~the~~ fourth aspect of the present invention, a method for a sense amplifier comprises steps of: forming a holding path including a main control switch and a holding switch; and providing an auxiliary control switch to control a turn-on and a turn-off of the holding path.

[0044] 9. A method for a sense amplifier, wherein the sense amplifier is the sense amplifier ~~as claimed in~~ according to embodiment 5, comprising steps of: