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Table with 5 columns: APPLICATION NO., FILING DATE, FIRST NAMED INVENTOR, ATTORNEY DOCKET NO., CONFIRMATION NO. Includes application details for Chung-Kuang Chen and examiner information for RADKE, JAY W.

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eoffice@volpe-koenig.com

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1. The present application is being examined under the pre-AIA first to invent provisions.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 11-17 are rejected under pre-AIA 35 U.S.C. 102b as being anticipated by Lee (US 2009/0323420 A1; hereinafter “Lee”).

Regarding claim 1: Lee (FIG. 8a, 8b, 9; [0055-0059]) teaches a sense amplifier, comprising:

a first switch (BLC transistor 840) having a first terminal (upper S/D terminal), a second terminal (lower S/D terminal) and a control terminal receiving a first bias (BLC);

a second switch (828) having a first terminal (upper S/D terminal) electrically connected to the first terminal of the first switch, a second terminal (lower S/D terminal) and a control terminal receiving a second bias (STB);

a third switch (826) having a first terminal (upper S/D terminal), a second terminal (lower S/D terminal) electrically connected to the first terminal of the first switch and a control terminal receiving a third bias (T2);

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a holding path including the second switch (the path through 828 and 832); and
a fourth switch (832) controlling a turn-on and a turn-off of the holding path and having a first terminal (upper S/D terminal) directly electrically connected to the second terminal of the second switch, a second terminal (lower S/D terminal) that is not directly electrically connected to a power supply or a common ground and a control terminal receiving a sensing signal (SEN 830).

Regarding claim 11: Lee (FIG. 8a, 8b, 9; [0055-0059]) teaches a sense amplifier comprising:

a switch circuit (FIG. 8a) having a main control switch (840), a sensing switch (826) and a holding switch (828), wherein the three switches have a first bias (BLC), a second bias (T2), and a third bias (STB) respectively; and

an auxiliary control switch (832) having a first terminal (upper S/D terminal) directly electrically connected to the holding switch to control an operation of the holding switch and a second terminal (lower S/D terminal) that is not directly electrically connected to a power supply or a common ground.

Regarding claim 12: Lee teaches the sense amplifier further comprising a sensing and pre-charging path including the main control switch (840) and the sensing switch (826), sensing a potential value of a storage cell connected to a bit line of a memory and generating a sensing signal (SEN 830) according to the potential value, wherein the

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switch circuit includes the main control (840), the sensing (826) and the holding (828) switches clamping the bit line according to the first to the third bias respectively.

Regarding claim 13: Lee teaches the sense amplifier further comprising a holding path including the holding switch (828) and the auxiliary control switch (832) electrically connected to the holding switch and receiving the sensing signal (SEN 830) to control a turn-on and a turn-off of the holding path accordingly.

Regarding claim 14: Lee teaches a sense amplifier according to Claim 12, wherein the memory is a flash memory (NAND string 712 is a type of FLASH memory).

Regarding claim 15: Lee (FIG. 8a) teaches a method for operating a sense amplifier comprising steps of:

forming a holding path including a main control switch (840) and a holding switch (828); and

providing an auxiliary control switch (832) having a first terminal (upper S/D terminal) directly electrically connected to the holding switch to control a turn-on and a turn-off of the holding path, and a second terminal (lower S/D terminal) that is not directly electrically connected to a power supply or a common ground.

Regarding claim 16: Lee (FIG. 8a, 8b, 9; [0055-0059]); teaches a method according to Claim 15 further comprising steps of:

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forming a sensing and pre-charging path including the main control switch (840) and a sensing switch (826);

sensing a potential value of a storage cell connected to a bit line of a memory via the sensing and pre-charging path ([0057-0058]); and

generating a sensing signal (SEN 830) according to the potential value.

Regarding claim 17: Lee teaches a method, wherein the step of providing an auxiliary control switch further comprising a step of controlling the turn-on and the turn-off of the holding path according to the sensing signal (SEN 830 drives the control gate of transistor 832, which is in series with 828; hence, controlling the turn-on and turn-off of the path through 828).

Allowable Subject Matter

4. Claims 2-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 2: The prior art made of record and considered pertinent to the applicant's disclosure, taken individually or in combination, does not teach or suggest the claimed limitation of the holding path pre-charges a memory in combination with the other limitations thereof as is recited in the claim.

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Regarding claim 3: The prior art made of record and considered pertinent to the applicant's disclosure, taken individually or in combination, does not teach or suggest the claimed limitation of the holding path pre-charges a memory and, when the second and fourth switches are turned on, the bit line is pre-charged to a first predetermined potential value in combination with the other limitations thereof as is recited in the claim. Claims 4-10 depend on claim 3.

Response to Arguments

5. Applicant's arguments with respect to claims 1-17 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY RADKE whose telephone number is (571)270-1622. The examiner can normally be reached on Monday-Friday 7:30AM-5:00PM EST, Alternate Fri off.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAY RADKE/
Examiner, Art Unit 2827

/HUAN HOANG/

Primary Examiner, Art Unit 2827