Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A system for generating a frame-displayable signal comprising;

a first VPU that comprises a processor and that receives an application signal in a format readable by the first VPU and processes the application signal to generate a first frame data signal;

a second VPU that comprises a processor and that receives an application signal in a format readable by the second VPU and processes the application signal to generate a second frame data signal; and

an interlinking module that processes the first and second frame data signals to generate a frame-displayable signal;

wherein the first and second VPUs communicate command and control signals with each other.

2. (Original) The system of claim 1, wherein the system is contained on a single card.

3. (Original) The system of claim 1, wherein the system is contained within two cards, one card for each VPU.

4. (Original) The system of claim 1, wherein the receipt of the application signal in a format readable by the first and second VPUs is done through first and second ring buffers.

5. (Original) The system of claim 1, wherein the command and control signals comprise first and second frame data signals.

6. (Original) The system of claim 1, wherein the step of processing the first and second frame data signals to generate a frame-displayable signal is done by the first VPU, which is a master to the second VPUs slave.

7. (Original) The system of claim 1, wherein a blackring receives the first and second frame data signals and:

compares a first pixel from the first VPU to information regarding the pixel color;

selects the first pixel from the first VPU when the color of the first pixel is different from the pixel color;

selects the second pixel from the second VPU when color of the first pixel matches the pixel color; and

merges the first and second frame data signals to generate the frame-displayable signal.

8. (Original) The system of claim 1, wherein the first and second VPUs are separate.

9. (Original) The system of claim 1, wherein the first and second VPU communicate by cable.

10. (Original) The system of claim 9, wherein the cable is detachable.

11. (Original) A video programming unit (VPU) system for generating a frame-displayable signal comprising;

a first VPU that comprises a processor and that receives an application signal in a format readable by the first VPU and processes the application signal to generate a first frame data signal;

a second VPU that comprises a processor and that receives an application signal in a format readable by the second VPU and processes the application signal to generate a second frame data signal; and

an interlinking module that processes the first and second frame data signals to generate a frame-displayable signal;

wherein the first and second VPUs communicate command and control signals with each other.

12. (Original) The system of claim 11, wherein the system is contained within two cards, one card for each VPU.

13. (Original) The system of claim 11, wherein the receipt of the application signal in a format readable by the first and second VPUs is done through first and second ring buffers.

14. (Original) The system of claim 11, wherein the command and control signals comprise first and second frame data signals.

15. (Original) The system of claim 11, further comprising a supercard that comprises the first and second VPUs.

16. (Original) The system of claim 11, further comprising a driver that generates the application signal as native format code readable by the first and second VPUs.

17. (Original) The VPU system of claim 15, further comprising a driver that generates an API signal received from an application programming interface that communicates between the driver and an application.

18. (Original) The VPU system of claim 11, further comprising first and second ring buffers that receive the application signal in a format readable by the first and second VPUs

19. (Original) The VPU system of claim 11, wherein the command and control signals comprise first and second frame data signals.

20. (Original) The VPU system of claim 11, wherein the first VPU is a master to the second VPUs slave, and wherein the first VPU processes the first and second frame data signals to generate a frame-displayable signal.